a mixer to mix the oscillator output with a second signal to produce a mixed signal; and

a phase detector outputting an error signal which is a function of a phase difference between the mixed signal and an input signal, the error signal being applied to the tuning input.

2. (Unchanged) The CMOS phase lock loop of claim 1 wherein the oscillator comprises a voltage controlled oscillator, the tuning input being responsive to a voltage of the error signal.

3. (Unchanged) The CMOS phase lock loop of claim 1 further comprising a bandpass filter to filter the mixed signal before being applied to the phase detector, the filtered mixed signal comprising a difference frequency between the tuned frequency of the oscillator output and a frequency of the second signal.

4. (Unchanged) The CMOS phase lock loop of claim 3 further comprising a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector.

5. (Unchanged) The CMOS phase lock loop of claim 1 further comprising a charge pump disposed between the phase detector and the oscillator.

6. (Unchanged) The CMOS phase lock loop of claim 1 further comprising a loop filter disposed between the phase detector and the oscillator.

7. (Unchanged) The CMOS phase lock loop of claim 1 wherein the oscillator comprises a voltage controlled oscillator, the tuning input being responsive to a voltage of the error signal, the CMOS phase lock loop further comprising a bandpass filter to filter the mixed signal before being applied to the phase detector, the filtered mixed signal comprising a difference frequency between the tuned frequency of the oscillator output and a frequency of the second signal, a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector,

a charge pump disposed between the phase detector and the oscillator, and a loop filter disposed between the charge pump and the oscillator.

8. (Unchanged) A complimentary metal oxide semiconductor (CMOS) phase lock loop, comprising:

a tunable oscillator having a tuning input;

a mixer coupled the oscillator; and

a phase detector having a first input coupled to the mixer, a second input adapted to receive an input signal, and an output coupled to the tuning input.

9. (Unchanged) The CMOS phase lock loop of claim 8 wherein the oscilator comprises a voltage controlled oscillator.

10. (Unchanged) The CMOS phase lock loop of claim 8 further comprising a bandpass filter coupled between the mixer and the first input of the phase detector.

11. (Unchanged) The CMOS phase lock loop of claim 10 further comprising a limiter coupled between the bandpass filter and the first input of the phase detector.

12. (Unchanged) The CMOS phase lock loop of claim 8 further comprising a charge pump coupled between the phase detector output and the tuning input of the oscillator.

13. (Unchanged) The CMOS phase lock loop of claim 8 further comprising a loop filter coupled between the phase detector output and the tuning input of the oscillator.

14. (Unchanged) The CMOS phase lock loop of claim 8 wherein the oscillator comprises a voltage controlled oscillator, the CMOS phase lock loop further comprising a bandpass filter coupled to the mixer, a limiter coupled between the bandpass filter and the first input of the

phase detector, a charge pump coupled to the phase detector output, and a loop filter coupled between the charge pump and the tuning input of the oscillator.

15. (Unchanged) A complimentary metal oxide semiconductor (CMOS) phase lock loop, comprising:

oscillator means for generating a first signal having a tunable frequency, the oscillating means comprising tuning means for tuning the frequency of the first signal;

mixer means for mixing the first signal with a second signal to produce a mixed signal; and

detector means for detecting a phase difference between the mixed signal and an input signal, and generating an error signal which is a function of the phase difference, the tuning means being responsive to the error signal.

16. (Unchanged) The CMOS phase lock loop of claim 15 wherein the oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal.

17. (Unchanged) The CMOS phase lock loop of claim 15 further comprising filter means for filtering the mixed signal before being applied to the detector means, the filtered mixed signal comprising a difference frequency between the tuned frequency of the first signal and a frequency of the second signal

18. (Unchanged) The CMOS phase lock loop of claim 17 further comprising means for limiting the filtered mixed signal from the filter means before being applied to the detector means.

19. (Unchanged) The CMOS phase lock loop of claim 15 further comprising means for sourcing current to the tuning means responsive to the error signal.